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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,202	09/10/2003	Akira Mochizuki	081848-0189	3238

22428 7590 03/23/2006

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/658,202	MOCHIZUKI, AKIRA	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/13/04, 10.24.03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/658202, file on 09/10/03.

Claim 1-6 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Podlesny et al. (US Patent 5657291).

3. As to claim 1, Podlesny et al. teach a register file comprising: a plurality of input ports each for receiving therethrough a write data and having a priority order specified among said input ports (see fig 2 fig 3 fig 4, summary, col 4 line 32 to col 5 line 46); and a plurality of registers each for storing therein said write data based' on a write address, each of said registers including an input port selector and a data storage for storing an output from said input port selector, said input port selector including a combinational circuit including a plurality of first AND gates each corresponding to one of said input ports and a first OR gate for generating a logical sum of outputs from said first AND gates (see fig 3 col 5 line 11 to col 7 line 60), wherein: each of said first AND gates in one of said input port selector receives a write instruction signal for specifying whether or not write data input through a corresponding one of said input ports is to be stored in a corresponding one of said registers, and generates a logical product of said write data and said write instruction signal and an inverted signal of each of said

write instruction signals received through said input ports each having a higher priority order compared to said input port corresponding to said one of said input port selector (see fig 3, fig 4 col 6 line 26 to col 8 line 52).

4. As to claim 2, Podlesny et al. teach further comprising a plurality output ports and a plurality of output port selectors each for corresponding to one of said output ports, wherein each of output port selectors includes second AND gates each disposed corresponding to one of said registers for generating a logical product of data stored in a corresponding one of said registers and an activating signal assuming a high level upon selection of said corresponding one of said register and a second OR gate generating a logical sum of outputs from said first e gates selector (see fig 3, fig 4 col 6 line 26 to col 8 line 52 and summary).

5. As to claim 3, Podlesny et al. teach wherein said data storage includes a synchronous D-FF including a master latch for latching an output from said first OR gate, and a slave latch for receiving data from said master latch (see col 6 line 48 to col7 line 61).

6. As to claim 4, Podlesny et al. teach wherein said write instruction signal is generated by a logical product of a decoded signal decoded from said write address to have bits in number corresponding to the number of said registers and a write enable signal specifying whether or not each of said input ports is allowed to write data (see col 7 line 60 to col 8 line 51).

7. As to claim 5, Podlesny et al. teach a register file comprising: a plurality of registers; a plurality of output ports each for delivering therethrough data stored in one of said registers specified by a read address (see fig 2 fig 3 fig 4, summary, col 4 line 32 to col 5 line 46); a plurality of read data selectors each corresponding to one of said output ports, each of said read data selectors including AND gates in number corresponding to said a number of registers and an

OR gate generating a logical sum of outputs from said AND gates, each of said AND gates generating a logical product of data stored in a corresponding one of said register and an activating signal which assumes a high level when said corresponding one said registers is specified (see fig 3, fig 4 col 6 line 26 to col 8 line 52).

8. As to claim 6, Podlesny et al. teach comprising the step of describing each of said read data selectors in a, design description so that said each of said read data selectors is implemented by a combinational circuit including said AND gates and said OR gate (see col 6 line 48 to col7 line 61).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is 571 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tat
Art unit 2825
March 2, 2005

THUAN DO
Primary examiner.
03/17/06